

CSE 244A (Section Id: 983558)

VLSI Test

Journal Article Presentation Panels

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Session 1: **Diagnosis**

Monday, November 25, 5:00 PM

- Zhiyuan Wang, Malgorzata Marek-Sadowska, K-H. Tsai, and Janusz Rajski, *Analysis and methodology for multiple-fault diagnosis*, in **IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems**, Volume 25, Issue 3, March 2006, Page(s):558-575. {Presenter: *Ritika*; Respondent: *Mingqi*}
- Jiang Brandon Liu and Andreas Veneris, *Incremental Fault Diagnosis*, in **IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems**, Volume 24, Issue 2, February 2005, Page(s):91-101. {Presenter: *Jie*; Respondent: *Fu*}
- Alberto Bosio, Patrick Girard, Serge Pravossoudovitch, and Arnaud Virazel, *A comprehensive framework for logic diagnosis of arbitrary defects*, in **IEEE Transactions on Computers**, Volume 59, Issue 3, March 2010, Page(s): 289-300. {Presenter: *Shanti*; Respondent: *Jonathan*}
- M. Sivaraman and A.J. Strojwas, *Path delay fault diagnosis and coverage - a metric and an estimation technique*, in **IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems**, Volume 20, Issue 3, March 2001, Page(s):440 - 457. {Presenter: *Justin*; Respondent: *Zhangheng*}

Session 2: **RTL Test**

Monday, November 25, 5:55 PM

- I. Ghosh and M. Fujita, *Automatic Test Pattern Generation for Functional Register-Transfer Level Circuits Using Assignment Decision Diagrams*, in **IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems**, Volume 20, Issue 3, March 2001, Page(s):402 - 415. {Presenter: *Girish*; Respondent: *Jie*}
- Andreas Riefert, Riccardo Cantoro, Matthias Sauer, Matteo Sonza Reorda, and Bernd Becker, *A Flexible Framework for the Automatic Generation of SBST Programs*, in **IEEE Transactions on Very Large Scale Integration (VLSI) Systems**, Volume 24, Issue 10, October 2016, Page(s):3055-3066. {Presenter: *Elakkia*; Respondent: *Shanti*}
- Elif Alpaslan, Yu Huang, Xijiang Lin, Wu-Tung Cheng and Jennifer Dworak, *On Reducing Scan Shift Activity at RTL*, in **IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems**, Volume 29, Issue 7, July 2010, Page(s):1110 - 1120. {Presenter: *Mila*; Respondent: *Rohit*}

Session 3: Adaptive Test

Wednesday, November 27, 5:00 PM

- Baris Arslan and Alex Orailoglu, *Aggressive Test Cost Reductions through Continuous Test Effectiveness Assessment*, in **IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems**, Volume 35, Issue 6, 2016, Page(s):2093-2103. {Presenter: *Fu*; Respondent: *Ritika*}
- Michihiro Shintani, Takumi Uezono, Tomoyuki Takahashi, Kazumi Hatayama, Takashi Aikyo, Kazuya Masu and Takashi Sato, *A Variability-Aware Adaptive Test Flow for Test Quality Improvement*, in **IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems**, Volume 33, Issue 7, July 2014, Page(s):1056 - 1066. {Presenter: *Imtiaz*; Respondent: *Xiao*}
- Ali Ahmadi, Haralampos-G. Stratigopoulos, Ke Huang, Amit Nahar, Bob Orr, Michael Pas, John M. Carulli and Yiorgos Makris, *Yield Forecasting Across Semiconductor Fabrication Plants and Design Generations*, in **IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems**, 2018. {Presenter: *Mingqi*; Respondent: *Mila*}

Session 4: Delay Test

Wednesday, November 27, 5:40 PM

- Ke Peng, Muhittin Yilmaz, Krishnendu Chakrabarty, and Mohammad Tehranipoor, *Crosstalk- and process variations-aware high-quality tests for small-delay defects*, in **IEEE Transactions on Very Large Scale Integration (VLSI) Systems**, Volume 21, Issue 6, 2013, Page(s):1129-1142. {Presenter: *Jonathan*; Respondent: *Imtiaz*}
- Mingjing Chen and Alex Orailoglu, *On Diagnosis of Timing Failures in Scan Architecture*, in **IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems**, Volume 31, Issue 7, July 2012, Page(s):1102-1115. {Presenter: *Ladislav*; Respondent: *Jindi*}
- Mahmut Yilmaz, Krishnendu Chakrabarty and Mohammad Tehranipoor, *Test-Pattern Selection for Screening Small-Delay Defects in Very-Deep Submicrometer Integrated Circuits*, in **IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems**, Volume 29, Issue 5, May 2010, Page(s):760 - 773. {Presenter: *Zhangheng*; Respondent: *Delvin*}

Session 5: Design for Test

Monday, December 2, 5:00 PM

- J. Rajski, J. Tyszer and N. Zacharia, *Test Data Decompression for Multiple Scan Designs with Boundary Scan*, in **IEEE Transactions on Computers**, Volume 47, Issue 11, November 1998, Page(s):1188 - 1200. {Presenter: *Xiao*; Respondent: *Justin*}
- Ismet Bayraktaroglu and Alex Orailoglu, *Concurrent Test for Digital Linear Systems*, in **IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems**, Volume 20, Issue 9, September 2001, Page(s):1132-1142. {Presenter: *Delvin*; Respondent: *Ladislav*}
- Yiorgos Makris, Ismet Bayraktaroglu, and Alex Orailoglu, *Enhancing reliability of RTL controller-datapath circuits via invariant-based concurrent test*, in **IEEE Transactions on Reliability**, Volume 53, Issue 2, June 2004, Page(s):269-278. {Presenter: *Jindi*; Respondent: *Girish*}
- Indradeep Ghosh, Anand Raghunathan, and Niraj K. Jha, *A Design-for-Testability Technique for Register-Transfer Level Circuits Using Control/Data Flow Extraction*, in **IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems**, Volume 17, Issue 8, August 1998, Page(s):706-723. {Presenter: *Rohit*; Respondent: *Elakkia*}